21. The semiconductor of Claim 1, wherein said sidewall entirely covers said gate electrode.

22. The semiconductor device of Claim 6, wherein said sidewall offset extends only towards one of said source and drain diffusion layers.

23. The semiconductor of Claim 6, wherein said sidewall entirely covers said gate electrode.

REMARKS

This paper is being provided in response to the May 16, 2001 Office Action for the above-referenced application. In this response, Applicant has amended the title, and amended Claims 1 and 6, and added new Claims 21-23 in order to more particularly point out and distinctly claim that which Applicant deems to be the invention. Applicant respectfully submits that the amendments to the Claims and the newly added Claims are supported by the originally filed specification.

In response to the objection to the title, Applicant has amended the title in accordance with remarks set forth in the Office Action. Accordingly, Applicant respectfully requests that this objection be withdrawn.

In response to the objection to Claim 6, Applicant has amended Claim 6 in accordance with remarks set forth in the Office Action. Accordingly, Applicant respectfully requests that this objection be withdrawn.

The rejection of Claims 1-4, 6, and 8-10 under 35 U.S.C. 102(b) as being anticipated by Cheng et al. (U.S. Patent No. 5,545, 575, hereinafter referred to as "Cheng") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1-4, 6, and 8-10, as amended herein, are neither disclosed nor suggested by Cheng.

Applicant's Claim 1, as amended herein, recites a semiconductor device having a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated, a gate electrode formed on the semiconductor substrate, a sidewall covering the gate electrode therewith, and drain and source diffusion layers formed at a surface of the semiconductor substrate around the gate electrode. The sidewall has a sidewall offset extending outwardly of the gate electrode along a surface of the semiconductor substrate in at least one of regions below which the drain and source diffusion layers are to be formed. The sidewall offset extends along a surface of a gate oxide film on which the gate electrode is formed. At least one of the drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset. Claims 2-4 depend from Claim 1.

Applicant's Claim 6, as amended herein, recites a semiconductor device having a semiconductor substrate, an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated, a gate

electrode formed on the semiconductor substrate, a sidewall covering the gate electrode therewith, and drain and source diffusion layers formed at a surface of the semiconductor substrate around the gate electrode. The sidewall has a sidewall offset extending outwardly of the gate electrode along a surface of the semiconductor substrate in at least one of regions below which the drain and source diffusion layers are formed. The sidewall offset extends along a surface of a gate oxide film on which the gate electrode is formed. Also included are low-resistive wiring layers that are formed at surfaces of the drain and source diffusion layers, the low-resistive wiring layers being located outwardly beyond a peripheral edge of the sidewall offset. At least one of the drain and source diffusion layers extending towards the gate electrode beyond an edge of the sidewall offset. Claims 8-10 depend from Claim 6.

Cheng discloses an insulated gate semiconductor device and method of manufacturing the same. (See Abstract). Disclosed in Figure 7 of Cheng is an arrangement of forming electrodes, which includes source region 57 and drain region 58, source region 59 and drain region 62. Openings are formed in a layer of dielectric material 63 to expose portions of 57, 58, 59, and 62, and portions 28 and 29 of gate electrodes 35 and 35'. Silicide 64 is formed on the exposed regions of 57, 58, 59, and 62 and on the exposed portions of 35 and 35'. An insulating layer 66 is formed on layer 63 and 64. Openings are formed in the layer 66 to expose portions of 64. (Col. 6, Lines 27-42). Also disclosed are dopant regions 57 and 58 having a concentration ranging from $1x10^{19}$ atoms/cm^3 to approximately $5x10^{20}$ atoms/cm^3. (Col. 6, Lines 1-4). Dopant regions 43 and 44 have concentration ranging between approximately $1x10^{16}$ atoms/cm^3 to approximately $5x10^{17}$ atoms/cm^3. (Col. 4, Lines 22-26).

Applicant's amended Claim 1 is neither disclosed nor suggested by Cheng in that Cheng neither discloses nor suggests ***a semiconductor device that includes a sidewall offset extending along a surface of a gate oxide film on which the gate electrode is formed***, as set forth in Applicant's amended Claim 1. Cheng discloses an insulating layer 66 formed on a layer of dielectric material and silicide 64, but neither discloses nor suggests a sidewall offset that extends along a surface of a gate oxide film, as in Applicant's amended Claim 1.

Applicant's Claim 6 is also neither disclosed nor suggested by Cheng for reasons similar to those set forth regarding amended Claim 1. In particular, Applicant's amended Claim 6 is also neither disclosed nor suggested by Chen in that Cheng neither discloses nor suggests ***a semiconductor device that includes a sidewall offset extending along a surface of a gate oxide film on which said gate electrode is formed***, as set forth in amended Claim 6.

In view of the foregoing, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of Claims 1-2, and 6-8 under 35 U.S.C. 102(b) as being anticipated by Kunishima et al. (U.S. Patent No. 5,316,977, hereinafter referred to as "Kunishima") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1-2 and 6-8 are neither disclosed nor suggested by Kunishima.

Applicant's Claim 1 is summarized above. Claim 2 depends from Claim 1.

Applicant's Claim 6 is summarized above. Claims 7 and 8 depend from Claim 6.

Kunishima discloses a semiconductor device and method of manufacturing the same. (See Abstract). In Figures 5A-5C, shown are steps for manufacturing an FET. (Col. 9, Lines 22-27). Figure 5C discloses an SiO_2 film 23 and a BPSG film 25 sequentially deposited on top of a substrate that is lamp annealed to increase the concentration of the p+ type impurity diffusion layer 17. Also included is $TiSi_2$ layer 21. (Col. 10, Lines 16-59; Figure 5C). Also disclosed in Figure 5A is a gate oxide film 5 and a gate electrode having stacked films. (Col. 9, Lines 32-35).

Applicant's Claim 1, as amended herein, is neither disclosed nor suggested by Kunishima in that Kunishima neither discloses nor suggests ***a semiconductor device that includes a sidewall offset extending along a surface of a gate oxide film on which the gate electrode is formed***, as set forth in Applicant's amended Claim 1. Kunishima discloses a gate oxide film 5, a gate electrode, and an arrangement that includes an SiO_2 film 23 and a BPSG film 25 sequentially deposited on top of a substrate. However, Kunishima neither discloses nor suggests ***a sidewall offset that extends along a surface of a gate oxide film on which the gate electrode is formed***, as in Applicant's amended Claim 1.

Applicant's Claim 6 is also neither disclosed nor suggested by Kunishima for reasons similar to those set forth regarding Claim 1.

In view of the foregoing, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of Claims 1-11 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Kunishima is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1-11 are neither disclosed nor suggested by the references taken separately or in combination.

Applicant's Claim 1 is summarized above. Claims 2-5 depend from Claim 1.

Applicant's Claim 6 is summarized above. Claims 7-11 depend from Claim 6.

Cheng and Kunishima are also summarized above. For reasons set forth elsewhere herein, Applicant respectfully submits that Claims 1 and 6 are neither disclosed nor suggested by Cheng and are also neither disclosed nor suggested by Kunishima, taken separately or in combination. The deficiencies of each of these references, discussed above, are not overcome by the other one of the references.

In view of the foregoing, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Applicant respectfully submits that newly added Claims 21-23 are also patentable over the cited prior art.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
HUTCHINS, WHEELER & DITTMAR

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Date

Donald W. Muirhead
Reg. No. 33,978

Patent Group
Hutchins, Wheeler & Dittmar
101 Federal Street
Boston, MA 02110